**FPGA: - Session 1**

|  |  |  |  |
| --- | --- | --- | --- |
| **A** | **B** | **C** | **Y** |
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 |

**O** Specification given by customer

Truth table:

**Y**

**a**

|  |  |  |  |
| --- | --- | --- | --- |
| 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 1 |

always @ (\*) begin

Y=(b&c)|(a&~c);

end

endmodule

**RTL/Verilog code:**

Module mux(a,b,c,y);

Input a,b,c;

Output reg y;

**Y=BC+AC’**

**Y=BC+AC’**

**B**

**C**

**A**

Circuit diagram:

K-map:

0

1

00 01 11 10

A

BC

**c**

**b**